REMARKS

Objections to the claims

Claim 1 has been objected to because lines 2 and 3, which currently recite "storing a second memory line not currently stored in the cache in place of the *second* memory line in the cache" should actually read "storing a second memory line not currently stored in the cache in place of the *first* memory line in the cache." Applicant apologizes for this error, and has corrected it by amendment.

Claim rejections under 35 USC 101

Claim 20 has been rejected under 35 USC 101 because it recites a modulated carrier signal, which has been deemed to be non-statutory subject matter. Applicant has amended claim 20 so that it does not recite a modulated carrier signal, and requests the withdrawal of this rejection.

Prior art rejections as to claims 1-9

Claim 1 is an independent claim, from which claims 2-9 ultimately depend. Claims 1-5 have been rejected under 35 USC 102(e) as being anticipated by Williams (2003/0110356). Claims 6-9 have been rejected under 35 USC 103(a) as being unpatentable over Williams in view of Chryson (6,549,930). Applicant submits that as amended, claim 1 is patentable over Williams alone as well as over Williams in view of Chryson. As such, claims 2-9 are patentable at least because they depend from a patentable base independent claim.

Claim 1 previously recited temporarily storing the second memory line to be stored in the cache in place of the first memory line (upon eviction of the first memory line from the cache) "in a buffer." Applicant has amended claim 1 to clarify this buffer. In particular, the buffer also stores "eviction data regarding the first memory line" (specification, p. 10, para. 41, ll. 3-4), as

well as "data resulting from conversion of the second memory line into a set of concurrently performable actions" (specification, p. 10, para. 40, ll. 6-7).

Applicant notes that there are advantages associated with temporarily storing the second memory line to be cached in a buffer that also stores eviction data regarding the first memory line and data resulting from conversion of the second memory line into a set of concurrently performable actions. In particular, utilization of such a buffer means that performance benefits associated with temporarily storing the second memory line can be achieved without having to add a buffer that exists solely for the purpose of temporarily storing the second memory line. Rather, this buffer can be, as described on page 6, lines 3-5 of the specification, "an existing buffer that is originally intended for a purpose other than temporary storage of [such] data." "[T]he use of an existing buffer to temporarily store memory lines to be cached, pending the eviction of other memory lines in the cache, allows for . . . performance benefits without increasing the resources needed by the system." (Specification, p. 11, para. 44, ll. 6-9.)

Applicant submits that Williams alone or in combination with Chryson does not teach, disclose, or suggest claim 1 as amended. As to Williams, the "fill buffer 12" that temporarily stores the second memory line in question does not also store eviction data regarding the first memory line and data resulting from conversion of the second memory line into a set of concurrently performable actions. In particular, Williams includes "write buffer 14" that appears to be dedicated for the purpose of storing eviction data regarding the first memory line, such that the "fill buffer 12" is dedicated for temporary storage of the second memory line in question. Chryson also does not disclose the same buffer that temporarily stores the second memory line also stores eviction data regarding the first memory line and data resulting from conversion of the second memory line into a set of concurrently performable actions. Chryson is indeed silent as to temporary storage of a second memory line to be loaded in place of a first memory line, and thus necessarily cannot disclose a buffer that provides for such temporary storage.

Therefore, claim 1 as presently recited provides advantages that Williams alone, or Williams in view of Chryson, cannot achieve. The performance benefits of temporarily storing a second memory line while waiting for a first memory line to be evicted are achieved in claim 1 "without increasing the resources needed" (specification, p. 11, para. 44, ll. 6-9), because the buffer that is already being used for storing eviction data regarding a first memory line and data resulting from conversion of the second memory line into a set of concurrently performable actions is also used for temporarily storing the second memory line. By comparison, Williams alone or in view of Chryson teaches a separate fill buffer 12 dedicated for the purpose of temporarily storing the second memory line. Therefore, Williams alone or in view of Chryson does not realize performance benefits "without increasing the resources needed," but rather realizes performance benefits *with* increasing the resources needed.

For these reasons, claim 1 is patentable over Williams and over Williams in view of Chryson.

Prior art rejections as to claims 10-17

Claim 10 is an independent claim, from which claims 11-17 ultimately depend. Claims 10-14 and 17 have been rejected under 35 USC 103(a) as being unpatentable over Williams in view of Applicant's Admitted Prior Art (APA). Claim 15 has been rejected under 35 USC 103(a) as being unpatentable over Williams in view of APA and further in view of Chryson. Claim 16 has been rejected under 35 USC 103(a) as being unpatentable over Williams in view of APA and further in view of Scaringella (5,890,219). Applicant submits that as amended, claim 10 is patentable over Williams in view of APA, Chryson, and/or Scaringella. As such, claims 11-17 are patentable at least because they depend from a patentable base independent claim.

Claim 10 previously recited temporarily storing the memory lines to be loaded into the caches "into one or more buffers." Applicant has amended claim 10 to clarify this. In particular, the buffers also store "eviction data regarding other memory lines to be evicted from the one or

more caches" (specification, p. 10, para. 41, ll. 3-4), as well as "data resulting from conversion of the memory lines into sets of concurrently performable actions" (specification, p. 10, para. 40, ll. 6-7).

Applicant notes that there are advantages associated with temporarily storing the memory lines to be cached in buffers that also store eviction data regarding other memory lines to be evicted from the caches and data resulting from conversion of the memory lines into sets of concurrently performable actions. In particular, utilization of such buffers means that performance benefits associated with temporarily storing the memory lines can be achieved without having to add buffers that exist solely for the purpose of temporarily storing the memory lines. Rather, these buffers can include, as described on page 6, lines 3-5 of the specification, "an existing buffer that is originally intended for a purpose other than temporary storage of [such] data." "[T]he use of an existing buffer to temporarily store memory lines to be cached, pending the eviction of other memory lines in the cache, allows for . . . performance benefits without increasing the resources needed by the system." (Specification, p. 11, para. 44, ll. 6-9.)

Applicant submits that Williams in combination with APA, Chryson, and/or Scaringella does not teach, disclose, or suggest claim 10 as amended. As to Williams in view of APA, the "fill buffer 12" that temporarily stores the memory lines in question does not also store eviction data regarding other memory lines to be evicted from the caches and data resulting from conversion of the memory lines into sets of concurrently performable actions. In particular, Williams in view of APA includes "write buffer 14" that appears to be dedicated for the purpose of storing eviction data regarding other memory lines, such that the "fill buffer 12" is dedicated for temporary storage of the memory lines in question. Chryson and Scaringella also do not disclose the same buffers that temporarily store the memory lines also store eviction data regarding the other memory lines and data resulting from conversion of the memory lines into sets of concurrently performable actions. Chryson and Scaringella are indeed silent as to temporary

storage of memory lines to be loaded in place of other memory lines, and thus necessarily cannot disclose buffers that provide for such temporary storage.

Therefore, claim 10 as presently recited provides advantages that Williams in view of APA, Chryson, and/or Scaringella cannot achieve. The performance benefits of temporarily storing memory lines while waiting for other memory lines to be evicted are achieved "without increasing the resources needed" (specification, p. 11, para. 44, ll. 6-9), because the buffers that are already being used for storing eviction data regarding the other memory lines and data resulting from conversion of the memory lines into sets of concurrently performable actions is also used for temporarily storing the memory lines. By comparison, Williams in view of APA, Chryson, and/or Scaringella teaches a separate fill buffer 12 dedicated for the purpose of temporarily storing the memory lines. Therefore, Williams in view of APA, Chryson, and/or Scaringella does not realize performance benefits "without increasing the resources needed," but rather realizes performance benefits *with* increasing the resources needed.

For these reasons, claim 10 is patentable over Williams in view of APA, Chryson, and/or Scaringella.

Prior art rejections as to claims 18-20

Claim 18 is an independent claim, from which claims 19 and 20 ultimately depend. Claims 18-20 has been rejected under 35 USC 102(e) as being anticipated by Williams. Applicant submits that as amended, claim 18 is patentable over Williams. As such, claims 19 and 20 are patentable at least because they depend from a patentable base independent claim.

Claim 18 previously recited temporarily storing the first memory line to be stored in the cache in place of the second memory line (upon eviction of the second memory line from the cache) "in a buffer." Applicant has amended claim 18 to clarify this. In particular, the buffer also stores "eviction data regarding the second memory line" (specification, p. 10, para. 41, ll. 3-4), as

well as "data resulting from conversion of the first memory line into a set of concurrently performable actions" (specification, p. 10, para. 40, ll. 6-7).

Applicant notes that there are advantages associated with temporarily storing the first memory line to be cached in a buffer that also stores eviction data regarding the second memory line and data resulting from conversion of the first memory line into a set of concurrently performable actions. In particular, utilization of such a buffer means that performance benefits associated with temporarily storing the first memory line can be achieved without having to add a buffer that exists solely for the purpose of temporarily storing the first memory line. Rather, this buffer can be, as described on page 6, lines 3-5 of the specification, "an existing buffer that is originally intended for a purpose other than temporary storage of [such] data." "[T]he use of an existing buffer to temporarily store memory lines to be cached, pending the eviction of other memory lines in the cache, allows for . . . performance benefits without increasing the resources needed by the system." (Specification, p. 11, para. 44, ll. 6-9.)

Applicant submits that Williams does not teach, disclose, or suggest claim 18 as amended. The "fill buffer 12" in Williams that temporarily stores the first memory line in question does not also store eviction data regarding the second memory line and data resulting from conversion of the first memory line into a set of concurrently performable actions. In particular, Williams includes "write buffer 14" that appears to be dedicated for the purpose of storing eviction data regarding the second memory line, such that the "fill buffer 12" is dedicated for temporary storage of the first memory line in question.

Therefore, claim 18 as presently recited provides advantages that Williams cannot achieve. The performance benefits of temporarily storing a first memory line while waiting for a second memory line to be evicted are achieved "without increasing the resources needed" (specification, p. 11, para. 44, ll. 6-9), because the buffer that is already being used for storing eviction data regarding a second memory line and data resulting from conversion of the first memory line into a set of concurrently performable actions is also used for temporarily storing the second memory

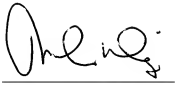
line. By comparison, Williams teaches a separate fill buffer 12 dedicated for the purpose of temporarily storing the first memory line. Therefore, Williams does not realize performance benefits "without increasing the resources needed," but rather realizes performance benefits *with* increasing the resources needed.

For these reasons, claim 18 is patentable over Williams.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mike Dryja, Applicants' Attorney, at 425-427-5094, so that such issues may be resolved as expeditiously as possible. For these reasons, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



January 9, 2007
Date

Michael A. Dryja, Reg. No. 39,662
Attorney/Agent for Applicant(s)

Law Offices of Michael Dryja
1474 N Cooper Rd #105-248
Gilbert, AZ 85233
tel: 425-427-5094
fax: 425-563-2098